AMENDMENTS TO THE SPECIFICATION:

I. Please modify the below paragraphs in the specification as follows:

[0023] FIG. 5A illustrates the schematic diagram of another embodiment of the shifter circuit apparatus of the invention that is capable of preventing floating input to its inverters;

[0039] However, a floating input to an inverter such as the inverter 441 directly fed by this node 203 may lead the inverter into a meta-stable status. Large current flows through an inverter in meta-stable mode, an undesirable situation. FIG. 5A shows another embodiment of the shifter circuit apparatus of the invention that is capable of preventing this situation. Another NMOS transistor 550 may be added which controllably connecting the node 203 to ground. This NMOS transistor 550 can be controlled by the same power-down control signal PWD that is fed to the gate terminal of the PMOS transistor 230 at node 231.

[0041] Note, however, that means other than NMOS device 550 can be employed as well to achieve the prevention of floating input to the inverter 441 of FIG. 5. For example, as shown in Fig. 5B, a simple resistor that is tied across the input of the inverter 441 (node 203) and ground may equally serve the same function. However, as is aware to those skilled in the art, the fabrication of an NMOS transistor for this purpose is not necessarily more complex and expensive than a resistor.

II. Please add the below new paragraph after paragraph 23 in the specification as follows:

[0023A] FIG. 5B illustrates the schematic diagram of still another embodiment of the shifter circuit apparatus of the invention that is capable of preventing floating input to its inverters;